

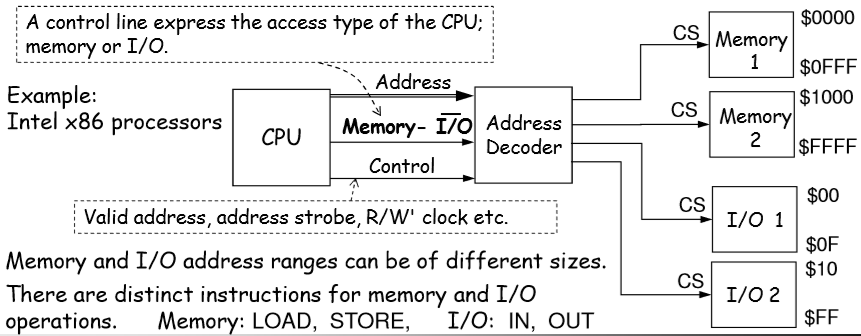
Instruction cycles of CPU:

1. Instruction Fetch Cycle
2. Operand Fetch Cycle
3. Execution Cycle
4. Interrupt Cycle

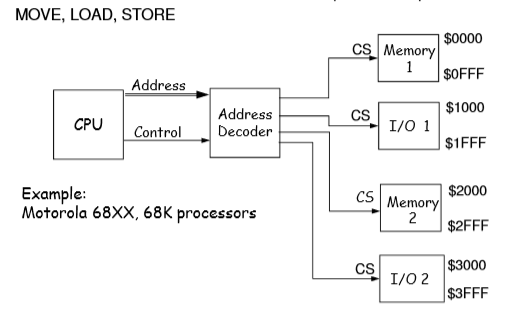
**CPU-IO CONNECTIONS:**

**1-Acording to the Adress Busses**

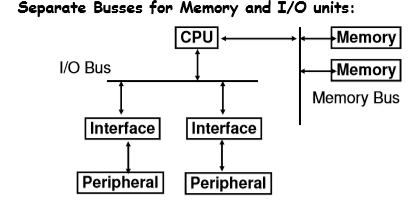
1. Isolated I/O Map: Seperated Adress Busses for memory and I/O

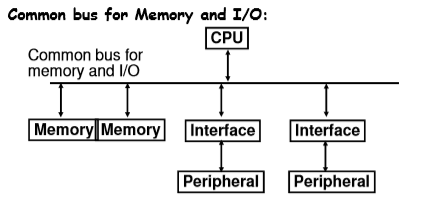


1. Memory Maped I/O: Same address space is shared by memory and I/O



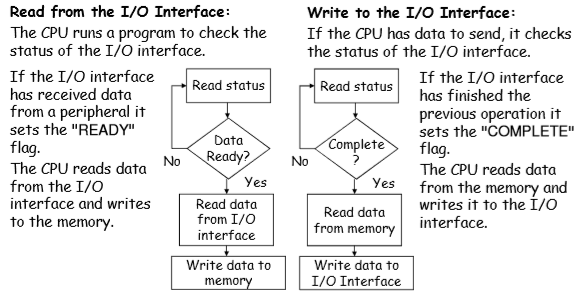
**2-Acording to the Data Busses**





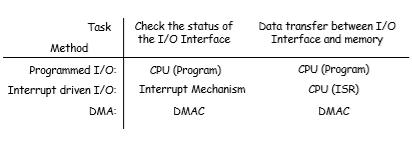
**DATA TRANSFER MODES BETWEEN I/O INTERFACES AND MEMORY:**

1. **Programmed I/O: It is the responsibility of the processor**
2. **Periodically check the status of I/O interface (ready, busy, complate)**
3. **To perform the data transfer betweeen memory registers and I/O interfaces.**



1. **Interrupt Driven I/O : In the interrupt driven technique the CPU sets the I/O interface to send an interrupt request if it is ready.**
2. **Direct Memory Access (DMA): In the programmed and interrupt-driven techniques the CPU is responsible for transfering data between memory and I/O interfaces. But here additional hardware modüle on the system bus called the DMA controller is responsible for transfering data between memory and I/O interfaces.**

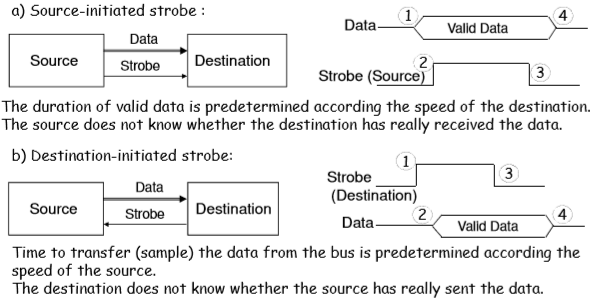
**COMPARISON BETWEEN 3 DATA TRANSFER MODES**

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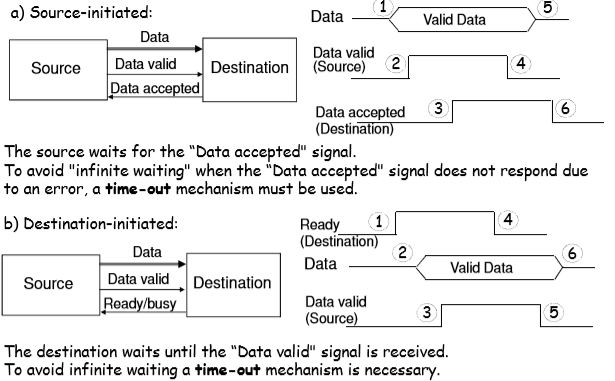
**ASYNCRONOUS DATA TRANSFER & SYNCRONOUS DATA TRANSFER**

**1-ASYNCRONOUS DATA TRANSFER:** The transfer is not syncronized with the clock.

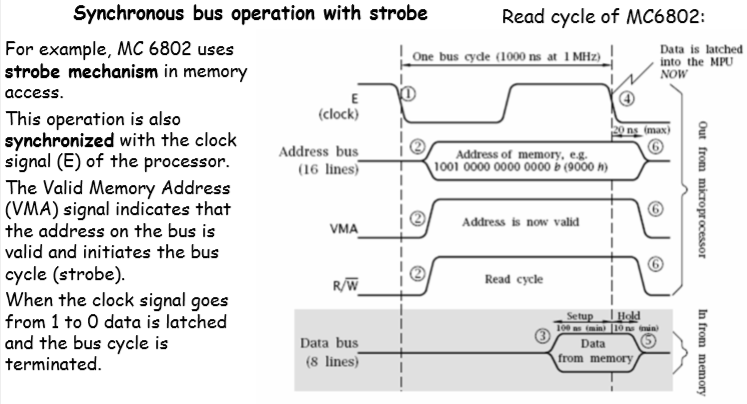
**1-a: Strobe Control**

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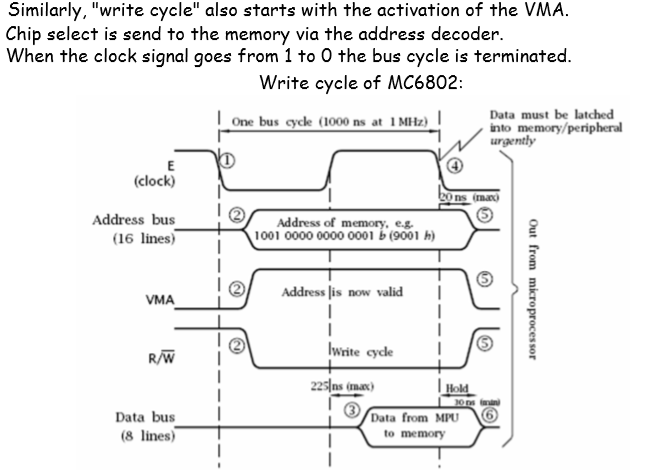
**1-b: Hand Shaking**

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**1-SYNCRONOUS DATA TRANSFER:** The transfer is syncronized with the clock (E).

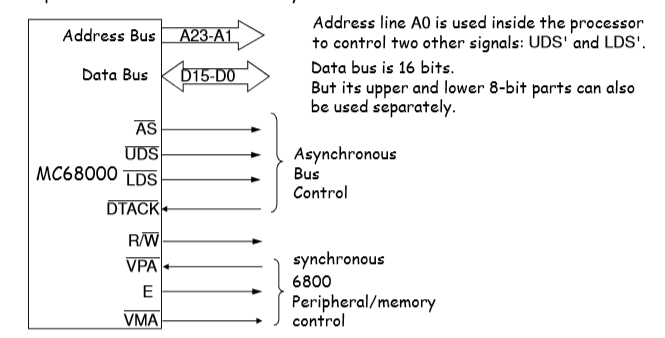


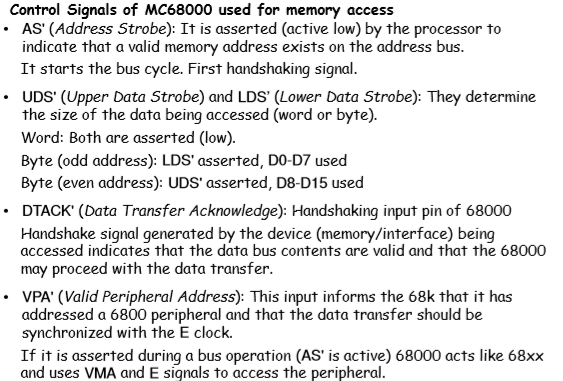
Here Adress bus, VMA(valid memory adress signal) and R/W’ control signal is sent to read data from memory as synchronous way.

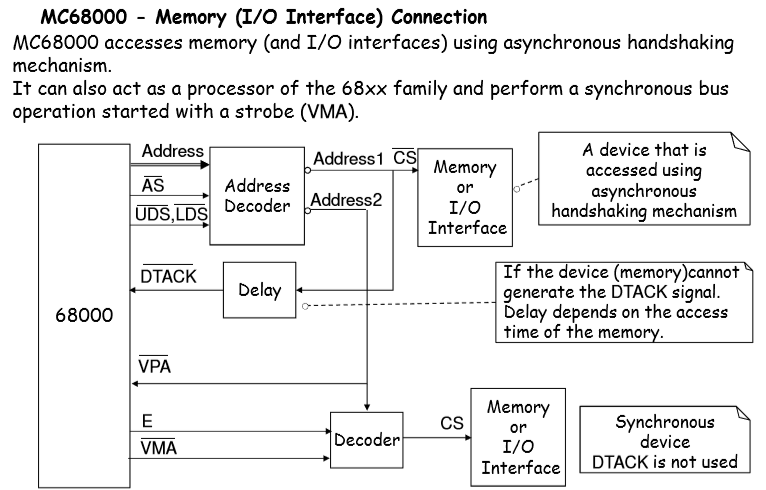


**Asynchronous bus operation with handshaking:**

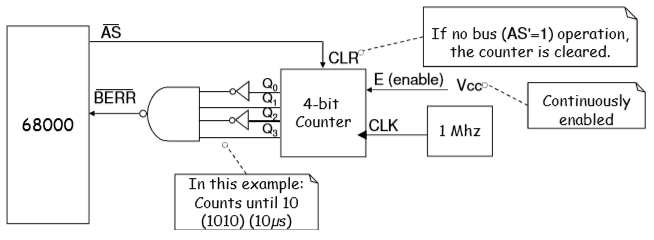
**MC68000 access the memory (and I/O interfaces) in both way (**syncronous and asyncronous**).**

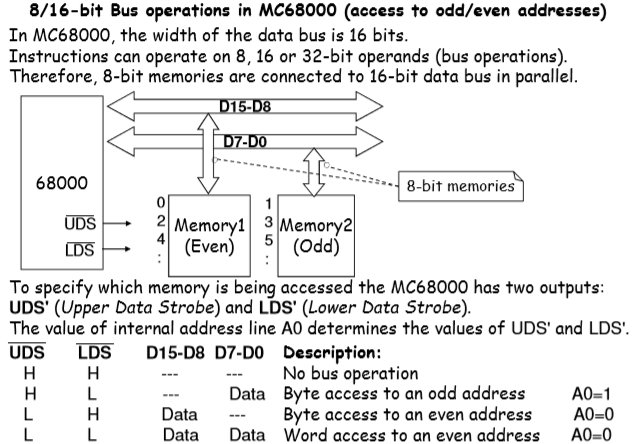


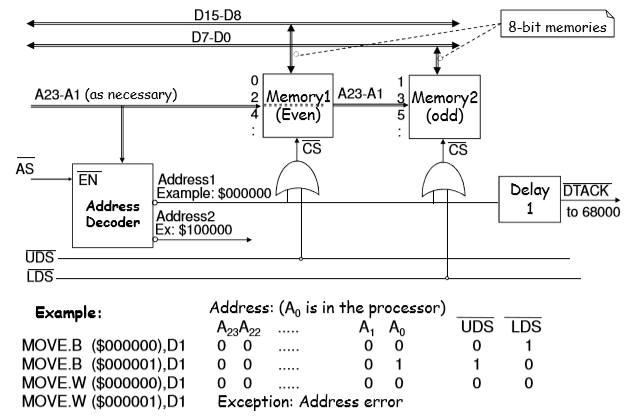




AVOIDING INFINITE WATING: In asyncronous comunication the computer sent AS’ signal and wait fort he DTACK. The DTACK should not be waited for infinite time.

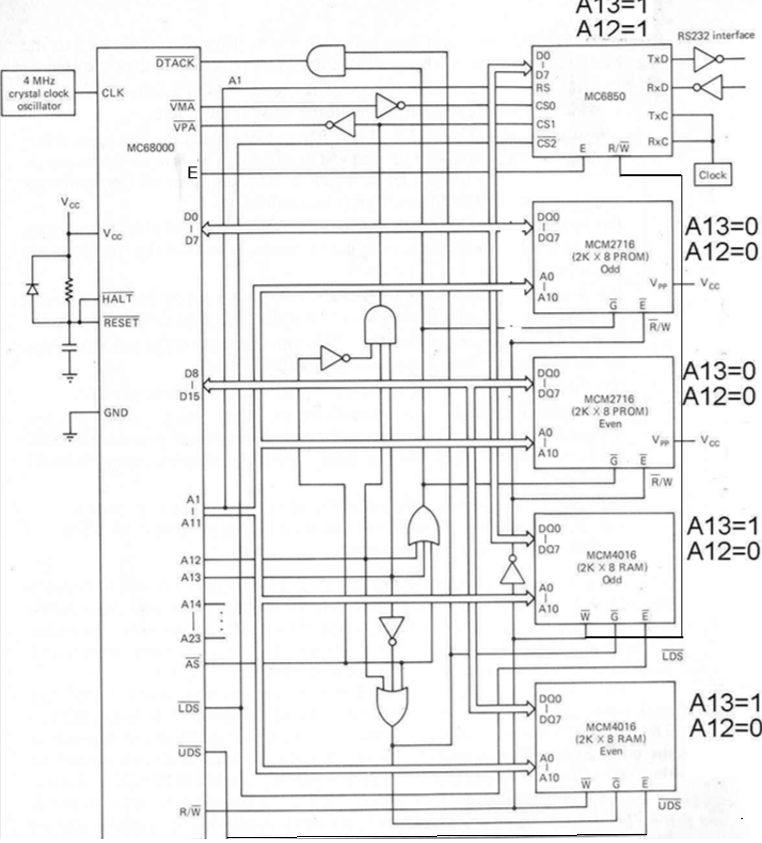


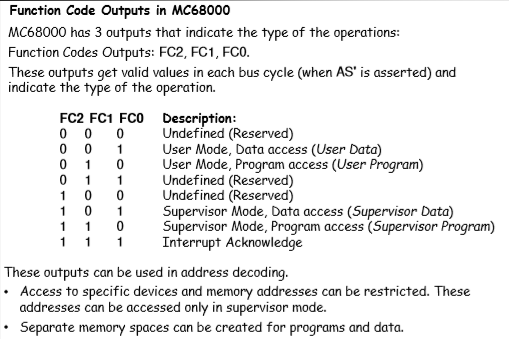


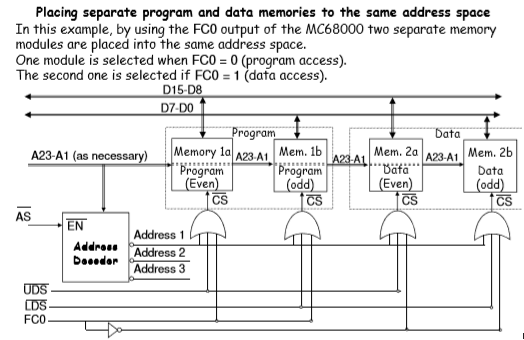


**EXAMPLE:**

In the example on the right following units are connected to the MC68000: One serial communication interface (MC6850), a total 4Kx8 ROM and total of 4Kx8 SRAM. Only two address lines A13 and A12 are used for address decoding. The serial communiction interface (MC6850) is connected as syncronous unit (VMA and E are used). There is asyncronous handshaking comunication between CPU and memories. (AS and DTACK is used). Since we dont write to ROMS UDS/LDS lines are not ued.



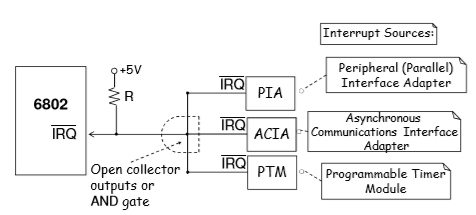




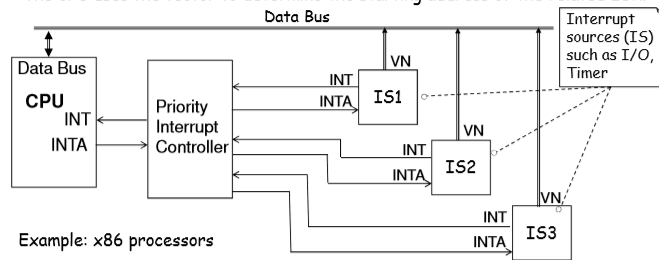
QUESTION:

There is a CPU that has 8 bits data bus and 16 bits adress bus. We want to add 4Kx8 RAM and 12Kx8 ROM (which contains three 4Kx8 ROM parts). The starting adress of RAM is $4000 and the starting adress of ROM is $F000. Draw the connections (data bus, adress bus, control bits, adress decoder part) between CPU and memories.

INTERRUPTS:

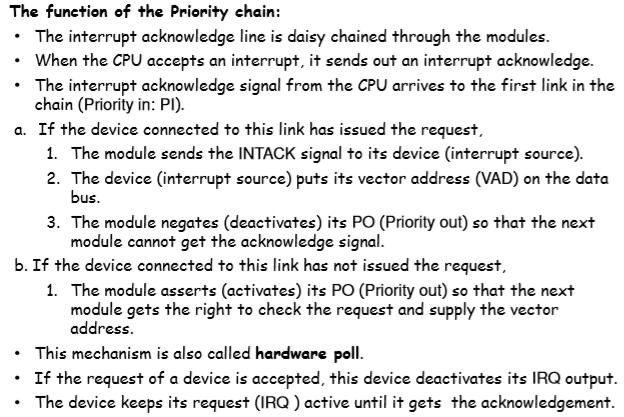


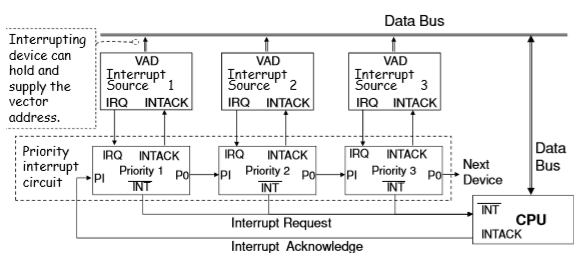
VECTORED INTERRUPTS



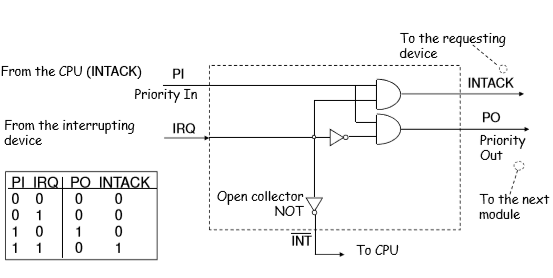
TO DECIDE THE PRIORITY:

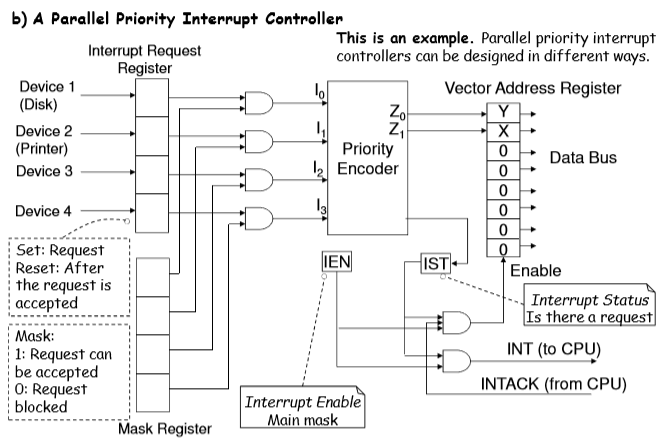
1-DAISY CHAIN:

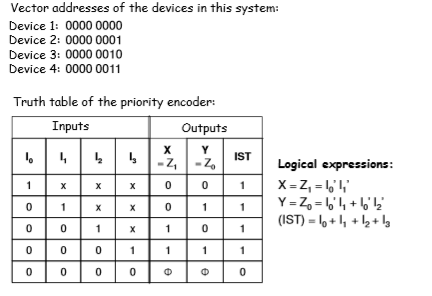




A cell of daisy chain







Interrupt Processing:

* Instruction Fetch Cycle
* Operand Fetch Cycle
* Execution Cycle
* Interrupt Cycle

Before entering the Interrupt cycle a processor should make some operation. If a request is accepted the CPU enters the interrupt cycle. In the interrupt cycle the following actions are performed by CPU. These are the internal oparations:

INTERRUPT SERVICE ROUTINE is the program that should be done fort he related operation of interrupt.

BEFORE ENTERING THE “INTERRUPT SERVICE ROUTINE (ISR)”

SP🡨SP-1

M[SP] 🡨PC (The current Program Cunter is writen to the stack)

INTACK🡨1 (CPU send the acknowladge signal to the I/O device that means the interrupt request is accepted)

PC🡨VAD (Vector adress of I/O Device)

SP🡨SP-1

M[SP] 🡨SR (The current Status Register is writen to the stack)

IEN 🡨0 (No more interrupt can be accepted)

|  |
| --- |
|  |
|  |
| SR |
| PC |
|  |

0004

0005

SPson🡪 0006

0007

SPilk🡪 0008

After PC took the I/O device instructon adress (VAD). The instructions related with I/O device is done. This program is called interrupt service routine.

RETURNING FROM THE “INTERRUPT SERVICE ROUTINE (ISR)”

SR🡨M[SP] (The previous Status Register value is read from the stack and is writen to SR)

SP🡨SP+1

PC🡨 M[SP] (The previous Program Counter value (previous instruction adress) is read from the stack and is writen to PC)

SP🡨SP+1

INTACK🡨0 (The communication with I/O device is finished.)

IEN 🡨1 (Interrupt can be accepted)